Impact of Alignment-Mark on Statistical Alignment Accuracy in E-beam lithography

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Outline

- Motivation
- New Alignment Mark:Design & Layout
- Experimental Results & Discussion
- Conclusion

Motivation

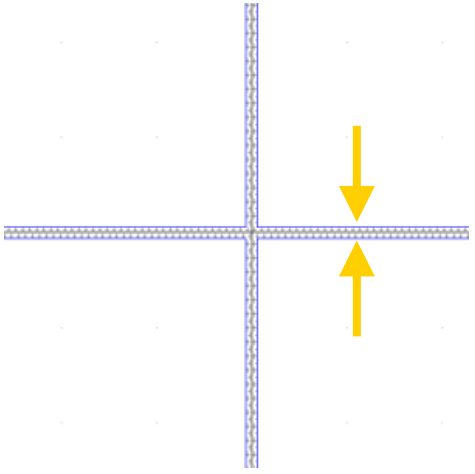
- Overlay accuracy of different mask levels increase.
- Due to the conventional CMOS process compatibility, materials for align-mark are limited (currently mesa-type $Si_{.50}Ge_{.50}$)
- However, mesa-type induces topology reducing subsequent process window (damaging align-mark)
- Goal:
  - Design align-mark to improve topology w/o increasing process complexity & compatibility

Design Approach

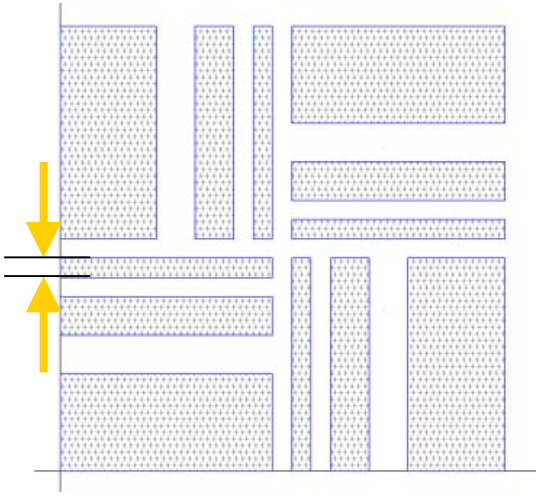
- Requirement:
  - Maintain conv. CMOS process & materials compatibility.
  - Improve subsequent process-window.
  - Better overlay accuracy (if possible).
- Type, Pattern Size & Shape
  - Trench-type
  - Size: 120nm, 250nm, 500nm
  - Shape: Cross, Compact square A, B

Layout

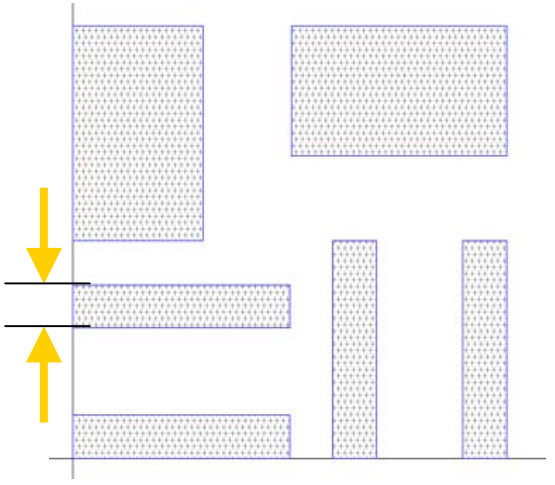
Cross-type



Square-type A

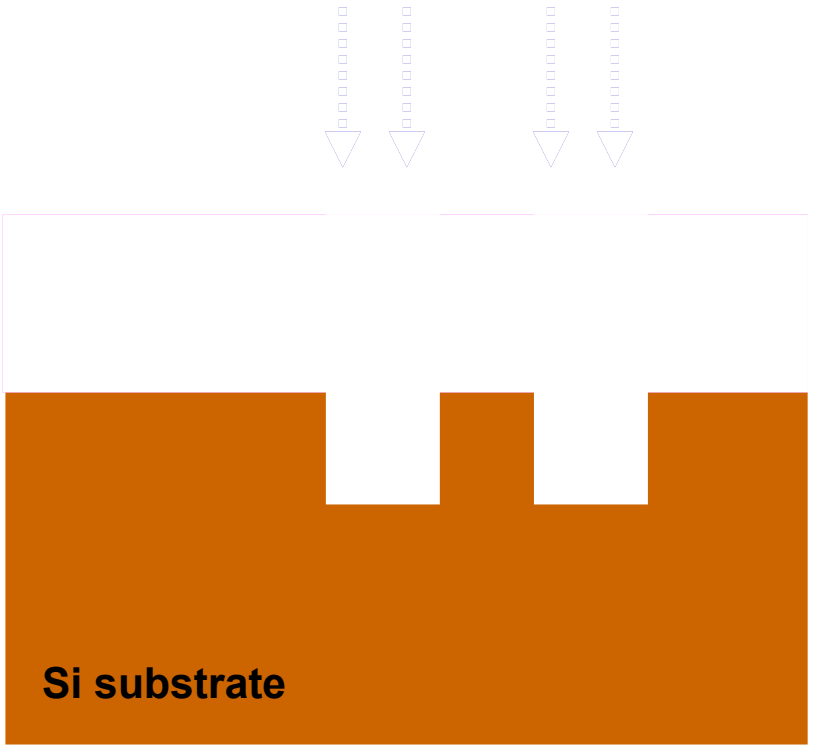


Square-type B



	Cross	Square-A	Square-B
Feature size	120/250/500 nm	120/250/500 nm	120/250/500 nm
Total area	400 μm^2	7/30/120 μm^2	1.4/6.3/25 μm^2

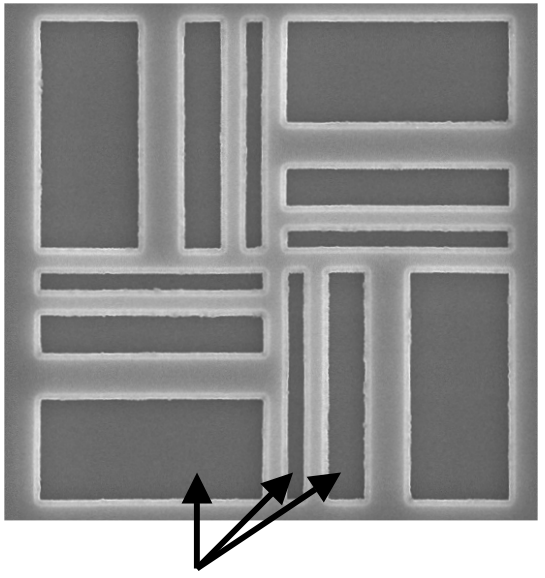
Fabrication Sequence



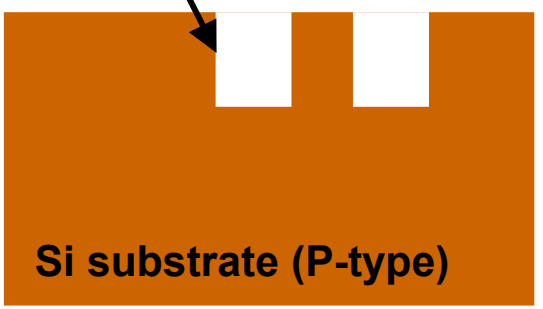
- Resist coating
  - KRS-XE (3000 rpm)
- Expose (dose split)
- Bake (1min 110^{o}C)
- Develop (30sec)
- Dry etching
  - Cl_2 + HBr (2min)
- Resist ashing

Fabrication Result

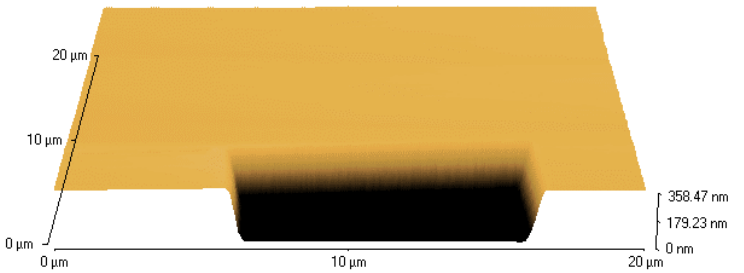
Plan-view SEM (type A)



Trench type



AFM Measurement

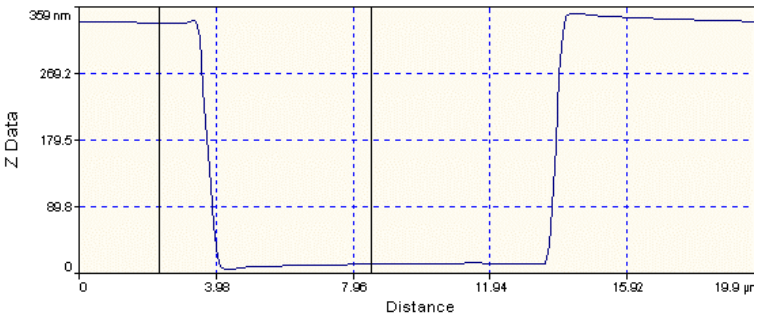


File Information:
Zmin: 0.0 nm Zmax: 358.5 nm Scan Range: 19 µm Resolution: 200 x 200

Result:

	Line1 X(µm)	Y(µm)	Z(nm)
Point1:	2.26	2.30	339.6
Point2:	8.51	2.30	13.8
Diff:	6.25	0.00	-325.8
Length:		6.259 µm	
Pt Angle:		2.98°	

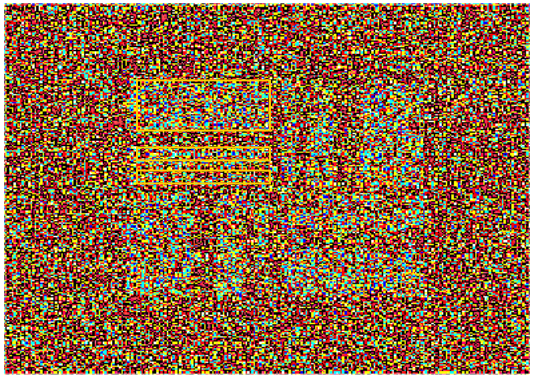
Depth = 358.5nm



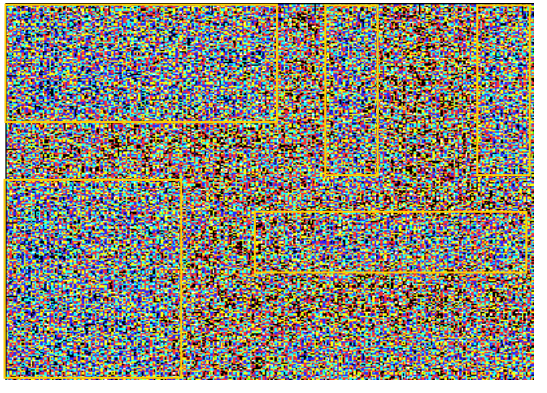
Alignment Test

Cross-type

Square-type A



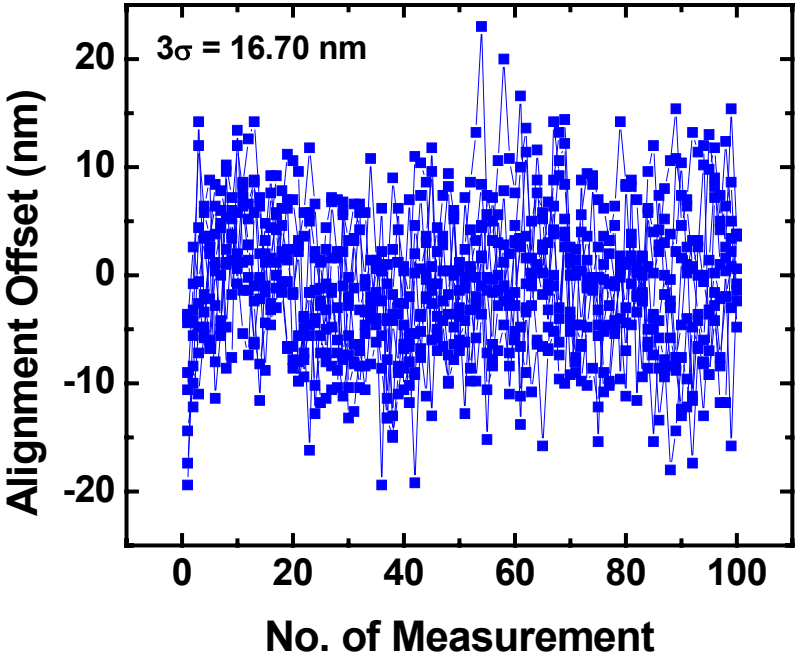
Square-type B



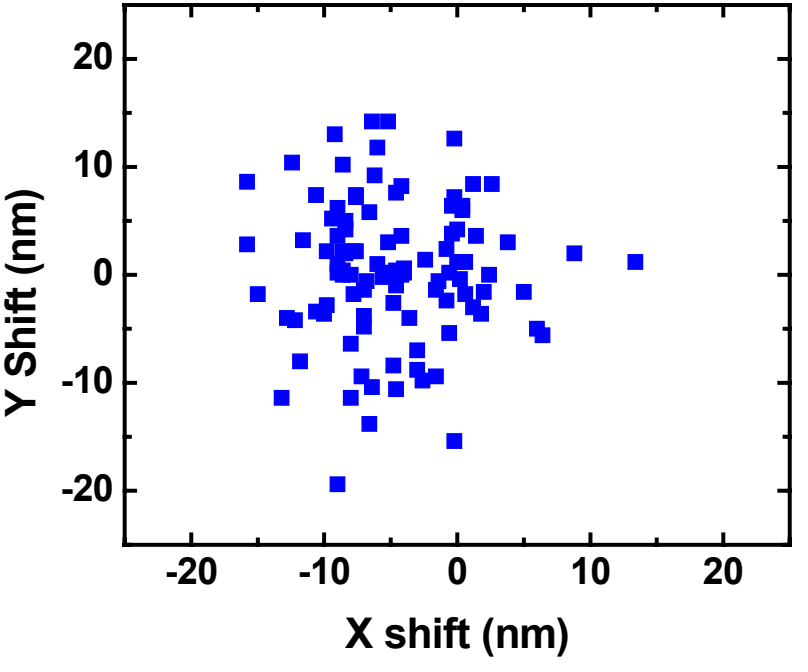
- Si Trench align-marks may be used in E-beam!
- Alignment accuracy?

Alignment Accuracy (I)

Statistical Measurement



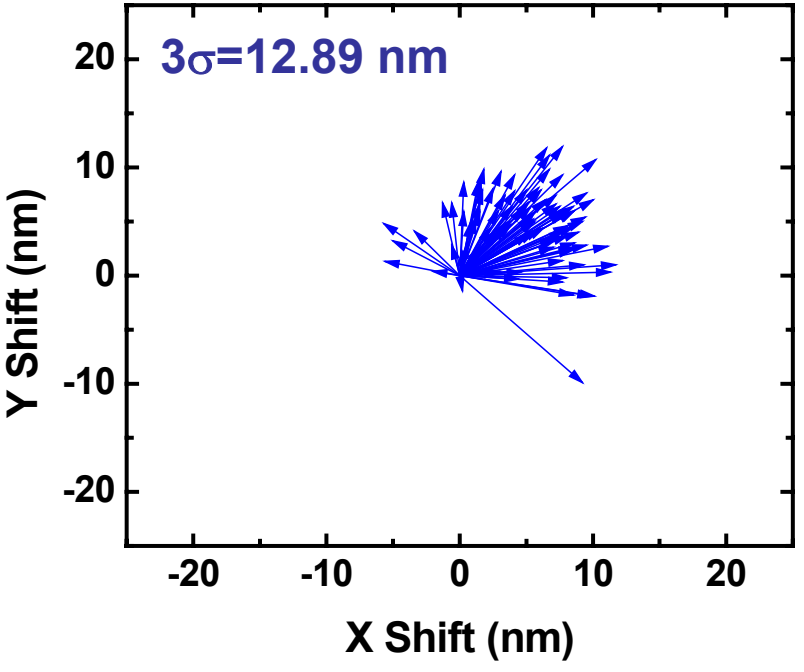
Correlation (x & y)



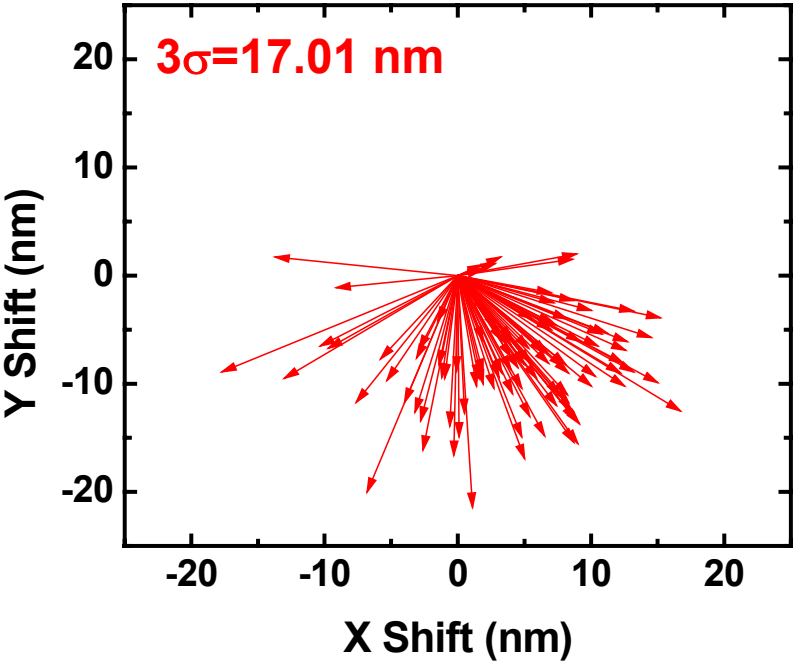
- Conv. cross-shape cannot be used.
- Accuracy ~ signal/noise

Alignment Accuracy (II)

w/o resist

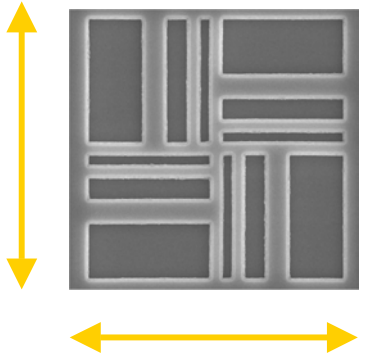


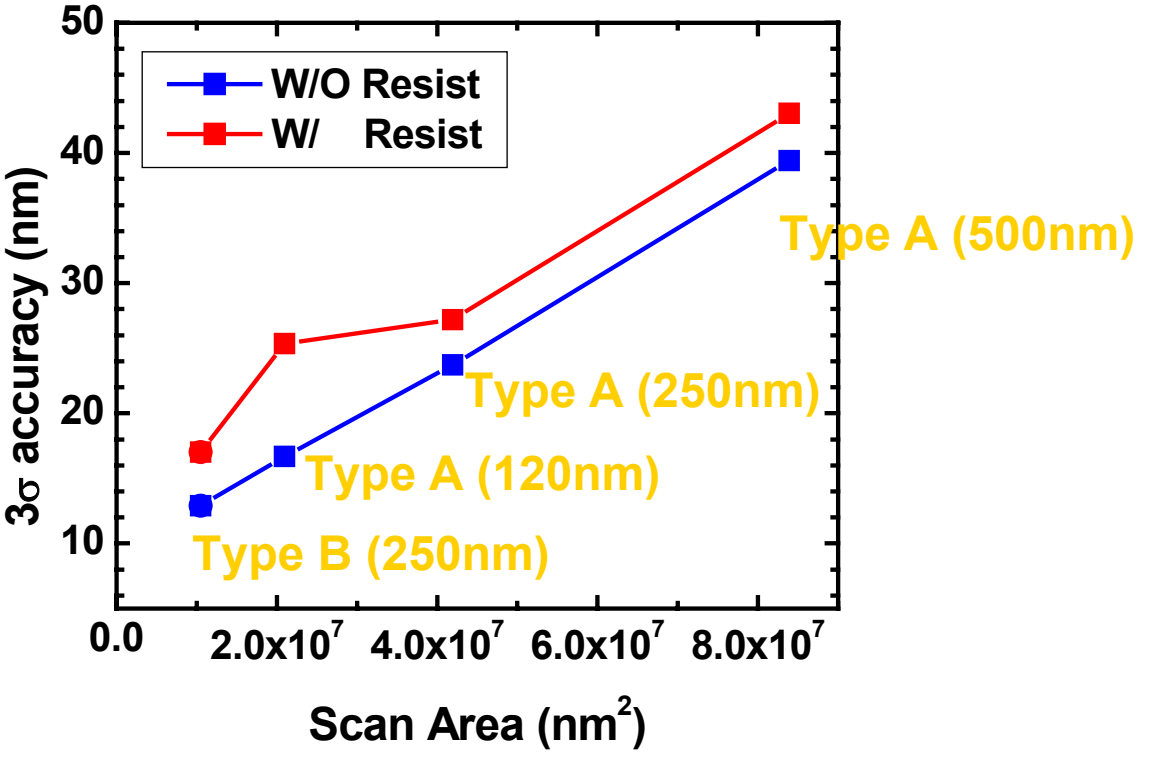
w/ AZPN resist



- w/ resist: accuracy degraded (noise increase)
- Reducing scan area?

Alignment Accuracy (III)





- Reducing align-mark area improve accuracy

Conclusion

- Si Trench align-marks can be used in E-beam. (CMOS process compatible, simpler process)

- Compact squares (type A, B)
  - ✓ achieve accuracy < 20nm (3 σ) [325x325μm^2]
  - ✓ show better immunity to noise.
  - ✓ save chip area.

- Future work
  - ➢ Effect of Trench depth
  - ➢ Optimize dimensions